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(54) **Sample and hold clock synthesis**

(57) A method and apparatus of correlated double sampling is disclosed by creating sampled and clamped signals from CCD imager outputs that are in phase with the CCD imager outputs comprising: providing an image sensor having an analog output; sensing the output of the image sensor via system electronics; identifying and extracting portions of a reset signal within the analog output signal; and modifying existing clocks in response to extracted portions of the reset signal.

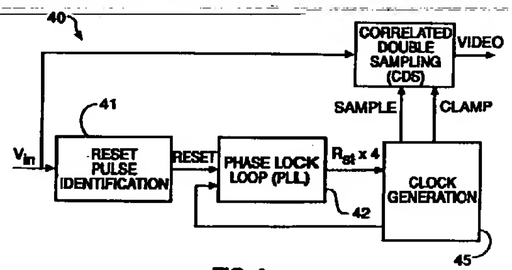

FIG. 4

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Description

Field of Invention

The invention relates generally to the field of imaging devices, and more particularly to the synthesis of sample and hold clocks used in correlated double sampling circuits.

Background Of The Invention

Semiconductor based imaging has become predominate for conversion of pictorial information into electronic data. Typically, charge coupled devices, CMOS based imagers, and other semiconductor based imagers are used in camcorders, still electronic cameras, fax machines, paper and film scanners.

The output of the semiconductor imager is an analog signal with four distinct "zones" of information. These zones, illustrated in Fig. 1, are characterized as reset, back porch, transition and video. The analog output of a semiconductor imager requires a sample and hold circuit to extract a more accurate representation of the video signal. Typically the sample and hold circuit is applied to the analog output of the semiconductor imager, before an analog to digital conversion can be performed. In these circuits the analog output of the semiconductor imager is the input to the sample and hold circuit. This signal is labeled V_{in} in Fig. 1 and displays the format of the video signal received from the image sensor. Sample and hold techniques that are applied digitally exist within the prior art. Such a teaching exists within U.S. Patent 5,086,344 issued to D'Luna et. al, which is commonly assigned with present invention. However, both analog and digital teachings within the prior art discuss voltage level adjustments rather than phase adjustment.

In most systems two sample and holds are used; one to clamp the "back porch" (V_{off}) and a second to sample the video (V_{sig}). These signals are subtracted to derive a more accurate video signal in what is often called Correlated Double Sampling (CDS). A larger magnitude difference indicates that more light has been detected.

A reset signal is used by the output stage of the imager to dump the charge associated with the previous output. This reset signal is capacitively coupled to the video output and typically leaves an artifact in the form of a positive pulse. For a CCD this pulse would be on the order of 100-600mV (V_{rst}). The rising edge of this pulse terminates the current output and the falling edge starts the next output.

Current art uses a single timing generator to create the reset, clamp and sample signals with the correct phase relationship to the analog video signal. There are timing requirements for minimum sample to reset delays, and reset to clamp delays. The system tolerance is typically added to these delays to guarantee that these requirements are met. This cumulative timing requirement typically results in a reduction of duty cycle for the clamp and sample pulses. Smaller pulses make it more difficult for the sample and holds to acquire the signals.

A typical system would have four separate ICs. If the propagation delay through each chip was known, the system could be designed to generate the proper phase relationship between the CDS pulses and the analog video. The problem is that the propagation delay is not constant between batches of chips, or over time and temperature.

The majority of the timing uncertainty occurs at the interfaces between chips. Each chip crossing might contribute a 5ns uncertainty. For three chip crossings, this would correspond to a total of 15ns worst case skew between the clamp sample pulses and the analog video. In fast systems the skew may be a significant portion of the total timing budget. At a pixel output rate of 20mhz, the sample window (T_{sa}) would be 50ns/4 or 12.5ns. If the system skew were 15ns, it would be impossible to build the system with the ability to properly adjust the signal delays in the system.

Tapped analog or digital delay lines could be used to delay the analog V_{in} or the digital clamp and sample pulses in the system. However, these delay line based systems require that various levels of calibration be performed. The level of calibration could easily vary and the calibration process would increase manufacturing cost and would not necessarily adapt to system variations resulting from temperature fluctuations and the aging process of the system.

If the sample pulse is not in the correct phase with the analog V_{in}, the sample and hold will acquire the signal on a sloping zone of V_{in} making the video signal extremely sensitive to clock jitter. Delay errors can greatly decrease the signal amplitude and make the system non-linear.

It should be apparent from the foregoing discussion that there remains a need in the art for devices and methods that will apply sample pulses to imager output signals in a manner that maintains proper phase relationships. This and other shortcomings within the prior art are addressed by the teachings of the present invention.

Summary Of The Invention

The present invention is directed to overcoming one or more of the problems set forth above. Briefly summarized, according to one aspect of the present invention, by identifying the artifact of the reset signal from the output of the semiconductor imager, V_{in}, which is input into a correlated double sampling unit, CDS, it is possible to create sample and clamp clock signals that have the ideal phase relationship to V_{in}. The identified reset pulse is then used to synthesize the CDS clocks or to modify existing CDS clocks.

By implementing this reset signal identification and CDS clock generation on the same integrated circuit, all

chip crossings associated with tolerance build up are removed. This has the added benefit of reducing by two the required number of interface pins between the CDS and the timing generator, potentially reducing package costs.

These and other aspects, objects, features and advantages of the present invention will be more clearly understood and appreciated from a review of the following detailed description of the preferred embodiments and appended claims, and by reference to the accompanying drawings.

Advantageous Effect Of The Invention

The present invention has the following advantages over the prior art: (1) it minimizes tolerance buildup on timing of the CDS clocks which results in easing system timing requirements; (2) it reduces the number of pins required to interface the timing generator to CDS by two pins; (3) it maximizes the video signal level by generating more accurate CDS clocks which results in higher speed operation; and (4) allows for wider clamp and sample clocks due to the minimized skew that is provided for by the present invention.

BRIEF DESCRIPTION OF TIE DRAWINGS

Fig. 1 is a diagram showing a sample of the window used in timing the video output from a semiconductor imager;

Fig. 2a is a diagram of a differentiator as employed by the preferred embodiment;

Fig. 2b is a diagram of a sample and hold circuit;

Fig. 3 is a block diagram of a CCD based imaging system with Correlated Double Sampling;

Fig. 4 is a diagram of a Correlated Double Sampling clock synthesis system as envisioned by the present invention;

Fig. 5 is a block diagram illustrating the usage of a phase lock loop as envisioned by the present invention; and

Fig. 6 is a diagram of an embodiment similar to that of Fig. 5 incorporating clock synthesis features on the phase lock loop.

To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures.

DETAILED DESCRIPTION OF TIE INVENTION

It has been discovered that the Reset Pulse within a video signal from a semiconductor imager can be identified through artifact within the video signal and used to provide a very exact phase relationship in sampling and clamping the video signal.

Referring to Fig. 1, which is a timing diagram for a typical video signal, generally referred to as V_{in} 11, that is output from an image sensor, there are several ways of identifying the reset pulse 12 from the V_{in} 11 signal shown in Fig. 1. It should be understood that the image sensor employed could be a charge coupled device as well as a CMOS base image sensor, or any image sensor having an analog output. There is reset artifact that exists only on the rising edge in the V_{in} 11 signal. By acquiring this reset artifact, it is possible to establish the proper phase relationship between the input signal, V_{in} 11, and the sample and hold circuit. A circuit as shown in Fig. 2a, known as a differentiator 21, could be used to generate a pulse on this rising edge of the video signal, V_{in} 11. The output from the image sensor is used as the input signal V_{in} 11, and filtered through capacitor, C1, and resistor, R1, prior to being input into differentiator 21. The difference between the filtered V_{in} 11 and a reference voltage level, V_{ref} 12, is magnified according to the parameters of differentiator 21. Capacitor, C2, and resistor, R2, provide the proper biasing for the correct feedback from the output of the differentiator 21 to the input of the filtered version of V_{in} 11. This is the most preferred method envisioned by the present invention of identifying the rising edge of video signal V_{in}.

Other sample and hold techniques are also envisioned by the present invention. Here, a comparator could be used to compare V_{in} to the CCD pedestal voltage (V_{off}) if known, however the pedestal voltage is not always known. Referring to Fig. 2b, which is a derivation of the comparator technique, if the clamping voltage, V_{clamp} were used instead of V_{in}, the comparison method could be simplified by comparing the clamping voltage V_{clamp} to the known V_{ref}. This would only synthesize the sample but not the clamp pulse. Another method would be to take the V_{in} level and compare it to an offset. Either a fixed voltage or a peak detector with a predetermined voltage removed from the peak detector as an approximation to V_{off}.

Fig. 3 is a block diagram of the various operations performed in a Correlated Double Sampling (CDS) System, generally referred to as 30. Here, CCD 32 receives incident light and outputs an analog video signal, V_{in} 11, to the CDS unit 34. A level shifter 31 will apply proper levels of reset and phase shit signal from the timing generator 35. The timing generator 35 will also supply clamp 21 and sample 22 signals to the CDS unit 34. The CDS unit 34 will output the corrected video signal to the analog to digital converters (A/D). It should be understood that the CDS 43 could be performed in digital rather than analog as shown in Fig. 3. In such a case that A/D would be performed prior to data reaching the CDS 43. It is also envisioned that such an embodiment could be performed with a digital PLL rather than an analog PLL.

Referring now to Fig. 4, which is a diagram of a Correlated Double Sampling clock synthesis system, generally referred to as 40, as envisioned by the present invention. Complete CDS clock synthesis 40 can be performed by a phase lock loop (PLL) 42 used to multiply the identified reset clock (as discussed above and generally referred to as sync 43) by a factor of four or

more. Other methods of multiplying the frequency of the sync signal are also envisioned. Among these would be Fuzzy Logic Controllers as well as various digital techniques. However the preferred embodiment employs phase lock loop technology because it employs more readily available technology. Since the sync pulse 43 has a duty cycle of ≤ 25%, it may be necessary to divide the sync pulse 43 frequency by two using a toggle flip-flop to create a 50% duty cycle signal for the PLL 42. Employing an analog device such as PLL 42 will typically generate a clock signal which is within 0.5ns of being completely in phase with the extracted reset clock. The PLL could be implemented in analog (phase discriminator and voltage controlled oscillator) or in digital using a base clock that has a higher frequency than the reset clock and phase resink technique to generate pulses that would effectively divide the frequency of the reset clock.

Fig. 5 is a block diagram of a phase lock loop based embodiment using off the shelf devices to create the phase lock loop (PLL) 42 as shown in Fig. 4. The phase lock loop 42 typically will contain a voltage controlled oscillator (VCO) 51, a phase discriminator 52, a prescaler 53 and a filter 54. The VCO will multiply its input by a factor of four. Prescaler 53 will divide the clock received from the VCO 51 by a factor of four. This divided clock is then input into the phase discriminator 52 along with the occurrence data related to the reset pulse from the reset identification 41. The phase discriminator 52 will properly adjust the phase relationship of the divided clock received from the prescaler 53, typically such that a rising edge of the divided clock will occur simultaneously with that of the identified rest signal. Filter 54 integrates the output of the phase discriminator 52 such that an average value of the output of the phase discriminator 52 is achieved. The filtered signal is then placed within VCO 51 which multiplies the signal by four to properly identify the quadrant of the video signal, V_{in}, input into clock generator 59, as previously discussed. In this manner unity is maintained by the phase lock loop. Employing off the shelf devices requires a separate phase lock loop 42 and clock generator 59.

Higher integration is desirable for the aforementioned reasons, including facilitating higher pixel readout rates. Referring to Fig. 6, which is a block diagram of the system employing the most preferred method of the present invention, that having phase lock loop (PLL), indicated by dotted line 142, integrated within the same device as the clock generator. The sample, clamp and sync signals are then all generated by the clock generator and prescaler unit 153. The remaining units within phase lock loop 142 perform the same functions as those previously discussed for Fig. 6.

If complete CDS clock synthesis is to be performed, either the sync pulse 43 or the output from the prescaler 53 is used as to indicate the start of a new pixel. If the reset (sync 43) frequency is multiplied by a factor of 4 (as shown in Fig. 1), the first (next) clock would be used to generate the clamp pulse and the third clock would be the sample pulse.

If only clock tuning is to be performed, the unmodified clamp and sample pulses are input to the clock generation block and the reset pulse is used to delay the start of the clamp pulse and to terminate early the sample pulse. This could be done by simply performing a logical AND of the clamp and sample pulses with the inverted reset pulse.

The sampling of V_{in} to generate the video signal may be done using a single sample and hold if the added accuracy of CDS is not required. There are many published methods for implementing sample and holds, all of which could be used in this system. Some notable styles are open loop, closed loop, FET switch and diode bridge.

Other features of the invention are included below.

The method wherein the step of modifying existing clocks in response to identified portions of the reset signal further comprises multiplying the frequency of reset clock with a phase lock loop.

The method wherein the reset signal frequency is divided half to enable the phase lock loop to lock upon it.

The apparatus wherein the synthesis means further comprises a phase-lock loop that synthesizes a pulse train used for generating the synthesized clocks.

The apparatus wherein the phase-lock loop is adaptive.

The apparatus wherein the phase-lock loop employs a Fuzzy logic controller.

The apparatus wherein the synthesis means is responsive to a plurality of outputs from the clock generator.

The apparatus wherein the image sensing device is a charge coupled device.

The apparatus wherein the synthesis means is responsive to a reset signal.

The apparatus wherein the synthesis means is responsive to a horizontal clock signal.

The apparatus wherein the means for sampling the image-bearing electronic signal further comprises means for performing a correlated double sampling.

The apparatus wherein the synthesis means further comprises means for generating a sample clock for sampling the image-bearing electronic signal and a clamping signal for generating a signal intended to capture a portion of the image-bearing electronic signal.

The apparatus wherein means for sampling the image-bearing electronic signal further comprises an analog to digital converter.

The apparatus wherein the analog to digital converter further comprises a convert input that identifies portions of the image-bearing electronic signal are to be parsed into discrete units under control of a convert clock from the synthesis means.

The apparatus further comprising a phase delay circuit within the synthesis means.

The apparatus further comprising a phase delay within the phase lock loop.

The device wherein the timing means further com-

prises a phase lock loop.

The device wherein the phase lock loop further comprises the output means on a single integrated circuit.

The device wherein the input signal is one of the following: a reset signal that is input to the device independently from the video signal; a reset signal that is derived from the video signal; or a horizontal clock signal that is input to the device independently from the video signal.

Claims

1. A method of creating sampled and clamped signals from CCD imager outputs that are in phase with the CCD imager outputs comprising the steps of:

   providing an image sensor having an analog output;
   sensing the output of the image sensor;
   identifying portions of a reset signal within the output; and
   modifying existing clocks in response to identified portions of the reset signal.

2. The method of claim 1 wherein the identifying step further comprises identifying the reset from a rising edge on the output and extracting a portion of the reset that coincides with a pulse generated at a predetermined point along the rising edge.

3. The method of claim 1 wherein the identifying step further comprises identifying the reset from by comparing the output with a predetermined voltage value and extracting a phase relationship of the reset signal relating to the output.

4. The method of claim 1 further comprising the step of indicating a start of a new pixel with the extracting portion of the reset signal.

5. A system for generating an electronic version of an image comprising:

   an image sensing device capable of converting light into an image-bearing signal representative of light incident upon the image sensing device, the image sensing device including a clock mechanism for transferring the image-bearing signal representative of light incident upon the image sensing device upon application of a clock stimuli;
   a clock generator for applying the clock stimuli to the image sensing device;
   synthesis means for generating a plurality of synthesized clocks to be employed for a sampling circuit, the synthesized clocks being partially decoupled from the clock generator; and
   means for sampling the image-bearing electronic signal in response to a sample pulse applied to the sampling circuit.

6. The apparatus of claim 5 wherein the synthesis means is responsive to the image-bearing signal.

7. The apparatus of claim 5 wherein the synthesis means is responsive to a clock which is generated by the image sensing device.

8. An integrated circuit device for generating control signals for a video signal comprising:

   an identification circuit for selecting a predetermined portion of the video signal in response to an input signal;
   timing means for providing synchronization between a selected portion of the input signal and the predetermined portion of the video signal;
   output means for generating a corrected video signal in response to the timing means.

9. The device of claim 8 wherein the output means further comprises a correlated double sampling unit.

10. The device of claim 8 further comprising:

   the timing means including a phase look loop with the capability of synchronizing phase between the input signal and a clock generated on board the phase look loop, and synthesis means for generating a plurality of synthesized clocks to be employed for a sampling circuit within the output means, the synthesized clocks being at least partially decoupled from a clock generator off the device used in generating the video.

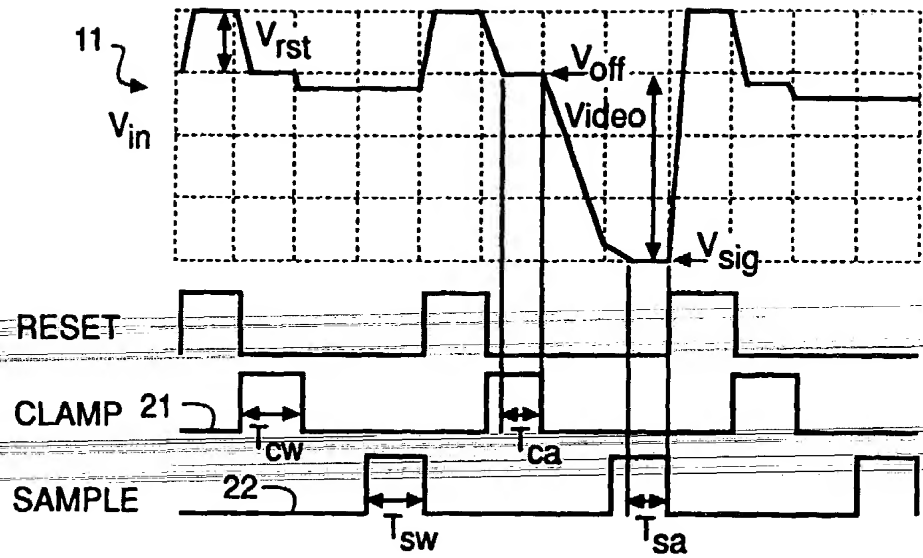
11
V_{in}
V_{rst}
V_{off}
Video
V_{sig}
RESET
CLAMP
21
T_{cw}
T_{ca}
SAMPLE
22
T_{sw}
T_{sa}

FIG. 1

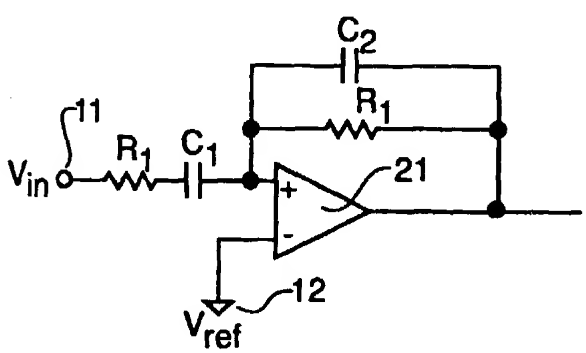
C_2
R_1
11
V_{in}
R_1
C_1
21
+
-
12
V_{ref}

FIG. 2

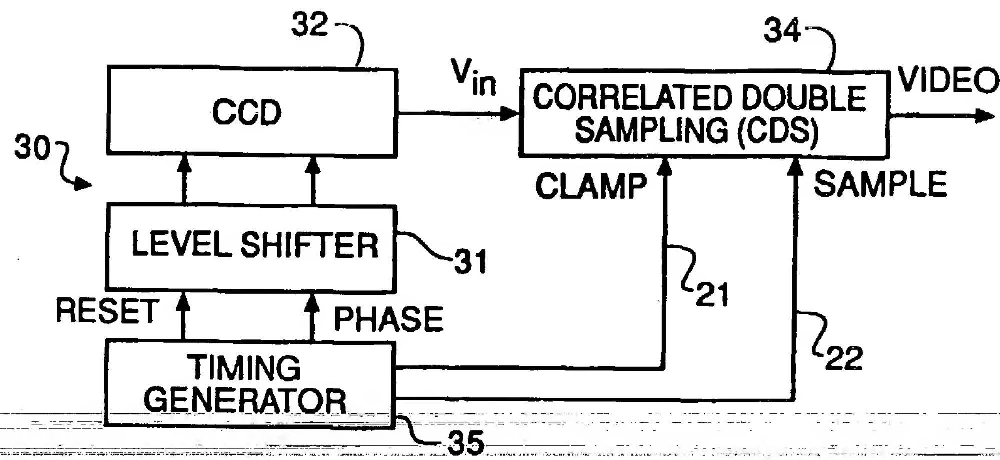
32
34
CCD
V_{in}
CORRELATED DOUBLE SAMPLING (CDS)
VIDEO
30
CLAMP
SAMPLE
LEVEL SHIFTER
31
21
RESET
PHASE
22
TIMING GENERATOR
35

FIG. 3

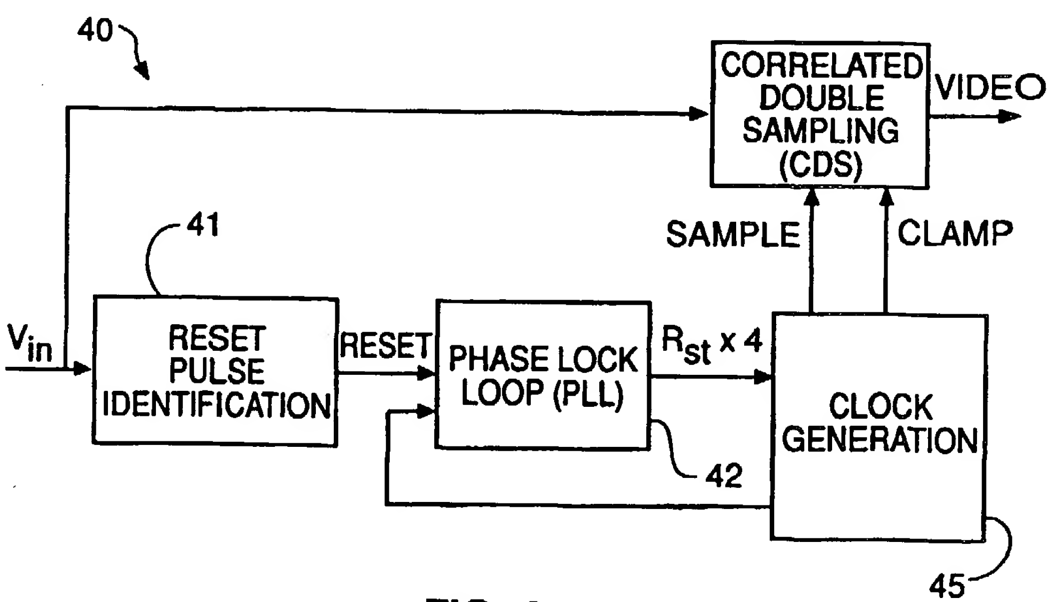
40
CORRELATED DOUBLE SAMPLING (CDS)
VIDEO
41
SAMPLE
CLAMP
V_{in}
RESET PULSE IDENTIFICATION
RESET
PHASE LOCK LOOP (PLL)
R_{st} x 4
CLOCK GENERATION
42
45

FIG. 4

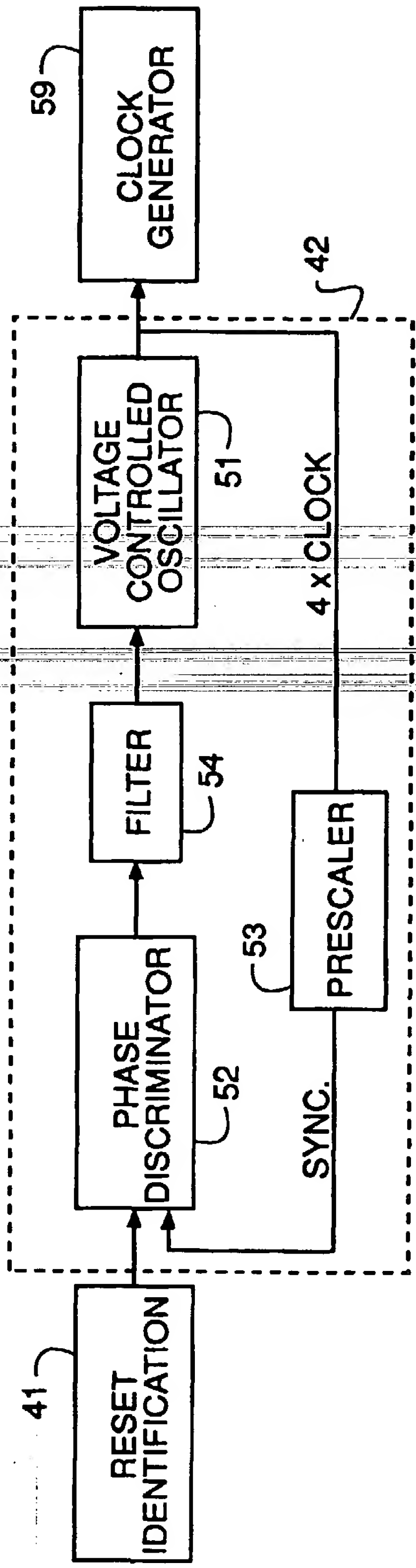
CLOCK GENERATOR
59
42
VOLTAGE CONTROLLED OSCILLATOR
51
4 x CLOCK
FILTER
54
PRESCALER
53
PHASE DISCRIMINATOR
52
SYNC.
RESET IDENTIFICATION
41

FIG. 5

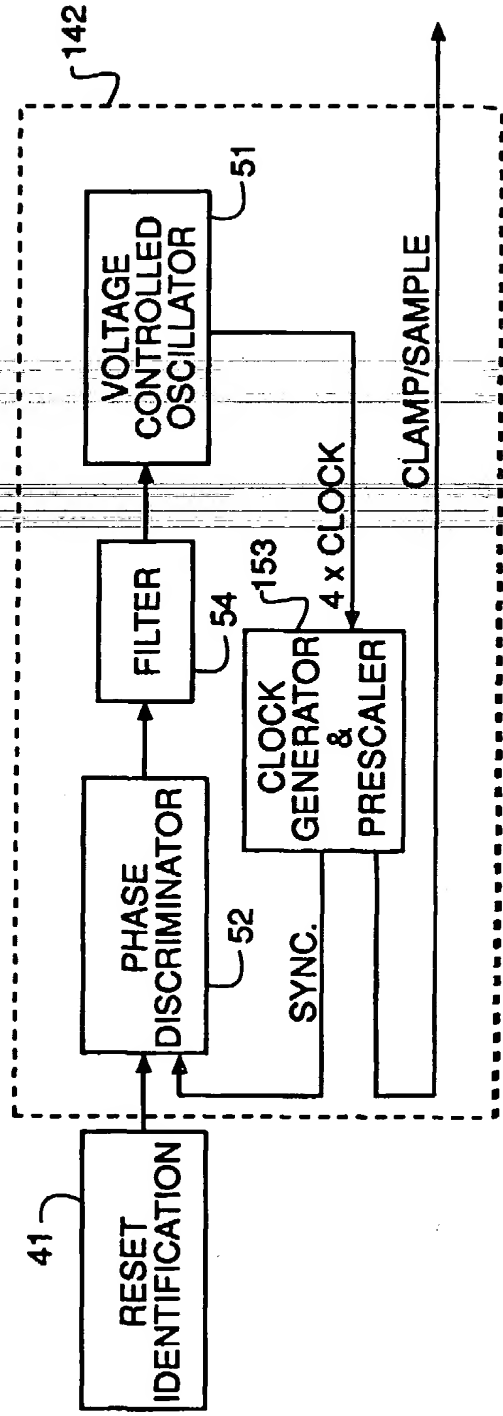
142
VOLTAGE CONTROLLED OSCILLATOR
51
CLAMP/SAMPLE
4 x CLOCK
153
FILTER
54
CLOCK GENERATOR & PRESCALER
PHASE DISCRIMINATOR
52
SYNC.
RESET IDENTIFICATION
41

FIG. 6